# Broadband passive RLGC(f) modeling for on-chip interconnect design

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*Abstract* – **To design state-of-the-art on-chip interconnect structures, efficient modeling tools are needed that accurately incorporate all substrate loss mechanisms and the finite conductivity and shape of the metallic interconnects. In this contribution, accurate broadband macromodels are conceived for the per unit length resistance (R), inductance (L), conductance (G) and capacitance (C) parameters of such on-chip interconnects. By means of adaptive frequency sampling (AFS) the simulation cost to obtain these models is small. Additionally, passivity can be assessed and enforced. The technique is applied to the analysis of an inverted embedded microstrip (IEM) line. Compared to commercial simulation software, both in frequency and time domain, excellent agreement and superior efficiency is observed, illustrating the method's applicability for on-chip design purposes.**

## 1 INTRODUCTION

The challenges in interconnect design are enormous. Ever more stringent design specifications in terms of bandwidth, speed, crosstalk, signal attenuation, etc., dictate the need for accurate models that can be easily used by circuit designers. Also, owing to further miniaturization, manufacturing tolerances play a significant role. Given all these constraints, it is of paramount importance that models are able to accurately incorporate the substrate loss mechanisms and the finite conductivity and shape of the metallic interconnects.

Often, interconnect structures can be characterized by using their cross-sectional geometry in a two-dimensional (2-D) electromagnetic (EM) simulation, leading to a corresponding multi-conductor transmission line model [1]. In particular, electrically long interconnects can be accurately described in terms of their per unit of length (p.u.l.) resistance (R), inductance (L), conductance (G) and capacitance (C) matrices. These models are usually denoted as RLGC(f) models, where the frequency-dependent character of the matrices is explicitly indicated. Many such transmission line models have been developed (see [1] and the references therein).

In the present contribution, the procedure described in [2] is used as a starting point. It makes use of the Dirichlet to Neumann (DtN) boundary operator and it complies with the above described requirements. The frequency-dependent behavior of the structures, due to the finite conducting metallic interconnects and the material parameters of the (doped) substrate(s), are accurately taken into account, and this from DC up to deep skin-effect frequencies.

However, the modeling tool described in [2] as such is not sufficient to be useful for state-of-the-art interconnect design. Thereto, a computer-aided design (CAD) environment that comprises accurate models which exhibit a guaranteed passive behavior over a very broad frequency range is imperative. Preferably, these models are compact and can be conceived in low CPU time. Therefore, in this contribution, the 2-D RLGC(f) models of [2] are improved upon by combining them with a number of techniques that have been proven useful in other research areas. One of these techniques, called vector fitting [3], [4], has been extensively used to calculate rational approximation models of linear systems, starting from tabulated frequency responses. It is shown here that this technique can be applied to compute a macromodel of the RLGC(f) data, allowing to replace the numerical RLGC(f) samples from the computationally expensive EM simulations by an analytic transfer function model. To compute this model in an efficient way, an adaptive frequency sampling (AFS) strategy [5] is applied to limit the overall simulation cost. The passivity of the model is assessed and enforced a posteriori when needed.

To illustrate the method presented here, we focus on a realistic application example, that is, an on-chip thin-film inverted embedded microstrip (IEM) line. After introducing the problem geometry at hand, the modeling procedure, consisting of two steps: (i) accurate RLGC(f) modeling via the DtN boundary operator and (ii) passive broadband macromodeling, is explained. Next, the IEM's frequency domain S-parameters are computed and compared with commercial simulation software. Also, time domain transmission (TDT) eye diagrams of a source-line-load configuration are calculated, demonstrating the method's applicability for on-chip design purposes.

## 2 INVERTED EMBEDDED MICROSTRIP (IEM) LINE

In this contribution we focus on on-chip interconnect structures, and more specifically, on an IEM. This particular interconnect topology, with a top-plate ground, gains importance in high-frequency

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IC-design [6] because it combines the advantages of classic microstrips (well-known modeling, smaller on-chip area needed than co-planar waveguide topology, etc.) with the availability of a nearly ideal (non-broken) ground plane. Here, we will investigate the IEM presented in Fig. 1. The build-up comprises a 500 µm doped silicon substrate with a relative permittivity $\varepsilon_r = 11.7$ and conductivity $\sigma = 20$ S/m, backed by a perfect electrically conducting (PEC) plane. On top of the silicon semiconductor, a 2.75 µm thick $SiO_2$ insulator with a relative permittivity $\varepsilon_r = 3.9$ is present. The IEM consists of a metallic strip with a width w = 20 µm, a thickness t = 0.1 µm, and a conductivity $\sigma_c = 4\ 10^7$ S/m, embedded in the $SiO_2$ 1.15 µm above the semiconductor. A PEC plate on top of the insulator serves as the ground plane of the microstrip line. This structure is very similar to the thin-film IEM presented in [7]. Here, however, a PEC top-plate ground is used to be able to rapidly simulate this structure using the 2.5-D full-wave solver Momentum of the Advanced Design System (ADS) from Agilent Technologies, Santa Rosa, CA, USA. As explained in [7], the IEM of Fig. 1 exhibits dispersive and slow-wave effects, making this structure interesting to investigate.

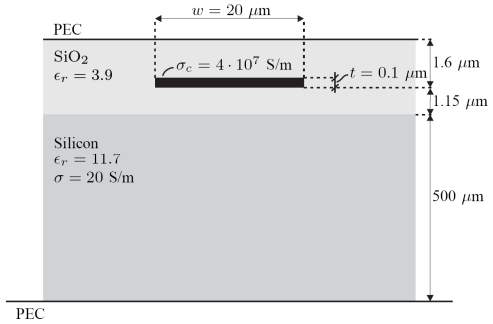



Figure 1: Material properties and geometrical details of the inverted embedded microstrip (IEM) line.

## 3 ACCURATE TABULATED RLGC(f) DATA COMPUTATION

In the recent past much attention has been paid to the accurate modeling of on-chip metal-insulator-semiconductor (MIS)-structures. Good modeling approaches must be able to predict the dielectric, the slow-wave, and the skin-effect modes, and therefore, it is crucial that the finite conductivities of all (semi)conductors are accurately taken into account.

In this contribution, the procedure described in [2] is adopted. This technique assumes a quasi-TM behavior of the fields and it is based on mode reciprocity rather than power conservation. For general MIS-structures, the complex capacitance problem is formulated to take semiconductors into account in the frequency range for which the semiconductor essentially behaves as a low loss dielectric. When the conduction current starts to dominate the semiconductor behavior, it is treated as an extra conductor. In that case a careful definition of the circuit currents still leads to a consistent formulation of the complex inductance problem. Solving the complex capacitance and inductance problem at a discrete number of frequencies, yields the *tabulated* p.u.l. resistance (R), inductance (L), conductance (G) and capacitance (C) matrices. Tackling these two problems is rather fast, since merely boundary integral equations (BIEs) have to be solved. These BIEs make use of (discretized) differential surface admittance matrices, obtained by invoking a discretized version of the DtN boundary operator.

## 4 EFFICIENT BROADBAND PASSIVE RLGC(f) MODELING

Although the above described technique is both accurate and already quite efficient in terms of CPU time, it can still be improved. Indeed, the result of the computation yields tabulated RLGC(f) data. First, it can be noted that in order to accurately capture broadband behavior of interconnects, many frequency samples have to be calculated, from DC up to several tens or evens hundreds of Gigahertz. Second, it is well-known that using tabulated RLGC(f) data does not guarantee passivity of the interconnect.

To deal with these two issues, the following approach is adopted. First, an AFS algorithm is applied to select a limited set of representative data samples that characterize the overall response of the system. Based on the selected RLGC(f) samples, the vector fitting algorithm computes an accurate pole-residue approximation of the data by solving successive least-squares problems in an iterative way. In a final step, the passivity conditions [8] are verified to assess the passivity of the model, and possible violations are corrected by a perturbation of the model coefficients [9].

The results are shown in Figs. 2 and 3, where the modeled R, L, G and C are plotted together with the original tabulated data from DC up to 320 GHz. A very good agreement is observed. Additionally, it is important to mention that R and L are described using two poles and to obtain this rational model only five frequency samples are needed. The model for G and C is a six-pole rational model, based on eight frequency samples. Computation of this limited number of samples and of the models themselves is very fast (see further, Table 1). On top of that, passivity is now guaranteed. This is imposed by demanding that all R, L, G, and C values are non-negative over the entire frequency band.

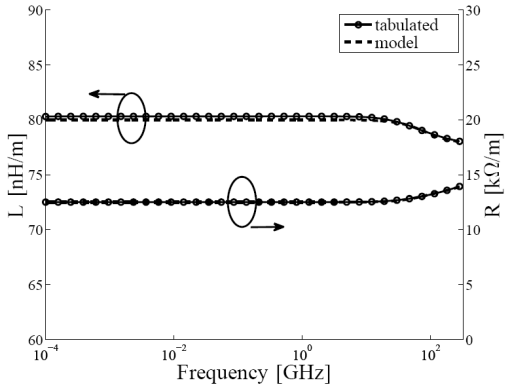



Figure 2: Tabulated and modeled p.u.l. inductance L and resistance R values of the IEM as a function of frequency.

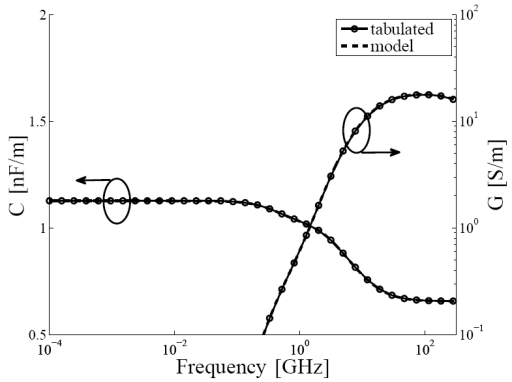



Figure 3: Tabulated and modeled p.u.l. capacitance C and conductance G values of the IEM as a function of frequency.

## 5 FREQUENCY AND TIME DOMAIN ANALYSIS OF THE IEM

Consider again the IEM with its cross-section as shown in Fig. 2 and now with a finite length of 1 mm. The frequency-domain characteristics of this line are investigated in terms of its S-parameters, i.e. its reflection ($S_{11}$) and transmission ($S_{21}$) coefficient, using 50 Ω as the reference impedance at both ports. A comparison is made between the results obtained by using (i) the tabulated data, (ii) the rational model, and (iii) simulations with ADS-Momentum. In Fig. 4 the amplitude of the reflection and transmission coefficient is presented. A very good agreement is observed between the tabulated and modeled data. Compared to ADS, only a small difference in transmission can be observed at higher frequencies, where $|S_{21}|$ is rather low. Obviously, also the phase of the S-parameters is important, and therefore the unwrapped phases of the reflection and transmission coefficient are shown in Fig. 5. Again a good agreement is observed.

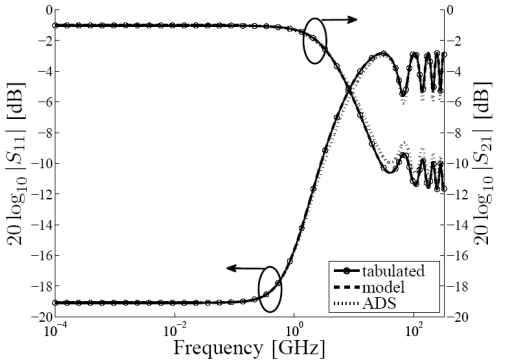



Figure 4: Magnitude of the reflection and transmission coefficient of the 1 mm long IEM.

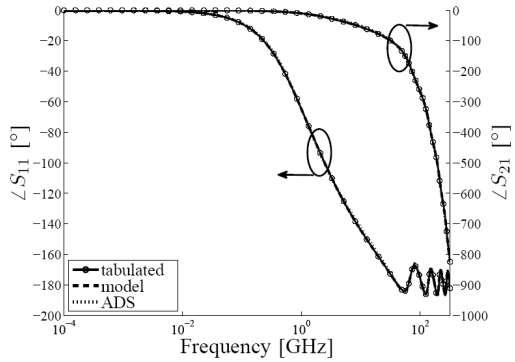



Figure 5: Unwrapped phase of the reflection and transmission coefficient of the 1 mm long IEM.

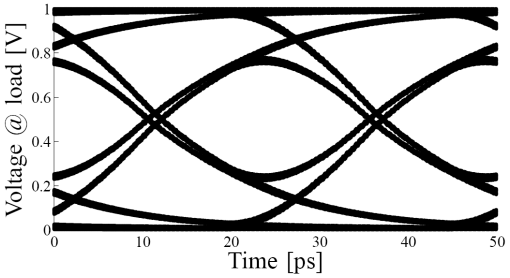
| Technique | Total elapsed time | Speed-up factor w.r.t ADS |
|---|---|---|
| *ADS* | 373.4 sec | |
| *tabulated model* | 13.9 sec | 26.9 |
| | 3.1 sec | 120.5 |

Table 1: Comparison of simulation times.

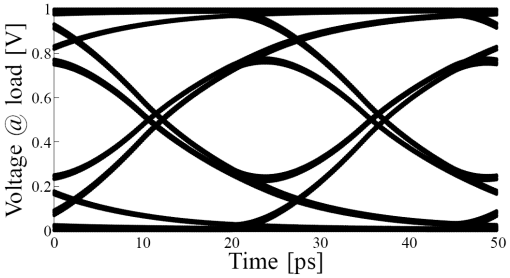
In addition to the accuracy, the efficiency of the modeling method is also considered. In Table 1 the total simulation time to compute the above S-parameters is shown. For all simulations a laptop (Dell Precision M4500, Intel(R) Core(TM) i7 X 940 @ 2.13 GHz with 8 GB of RAM) was used. Computing the tabulated data is in essence solving a 2-D problem, and is much faster than a full-wave simulation in ADS. To calculate the S-parameters from the tabulated data, 100 frequency samples were used. Thanks to the AFS, far less samples were needed to conceive the rational models. Building the rational models from these samples only takes about one second, leading to a low overall simulation time.

The S-parameters completely describe the IEM and hence, from the above, the proposed method is validated and its accuracy and efficiency are demonstrated. Nevertheless, for a chip designer, time domain results and TDT eye diagrams in particular,

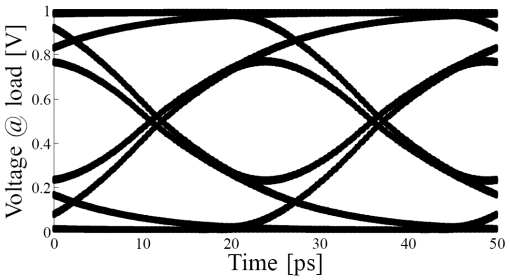
provide valuable information. Therefore, consider now a low impedance generator, consisting of a voltage source in series with a 1 Ω resistor, driving the 1 mm long IEM that is terminated by a capacitive load of 1 pF. The generator produces a pseudo-random bit sequence at a bitrate of 40 Gbps, a rise and fall time of 15 ps, and a voltage swing of 1 V. The resulting TDT eye diagrams are shown in Fig. 7, demonstrating again excellent agreement.



(a) Results obtained using tabulated RLGC(f) data.



(b) Results obtained using the rational model.



(c) Results from ADS.

Figure 7: TDT eye diagrams.

## 6 CONCLUSIONS

A new modeling method for state-of-the-art on-chip interconnect structures is presented. Starting from accurate but tabulated p.u.l. RLGC(f) data, obtained via a DtN boundary operator technique, compact macromodels are built, maintaining the needed precision. An improved efficiency is achieved by invoking AFS. Additionally, passivity can be assessed and enforced. The technique is applied to an on-chip IEM line, for which the substrate losses and the finite conductivity and shape of the metallic interconnect play a significant role. Comparisons were made with commercial simulation software, both in frequency and time domain, leading to the conclusion that the presented method is very accurate and also exhibits superior efficiency, making the technique very suitable for on-chip design purposes.

**Acknowledgments**

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