Recent Trends in the Integration of Circuit Optimization and Full-Wave Electromagnetic Analysis

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Invited Paper

***Abstract*—In this paper, we provide an overview of some recent trends for the general electromagnetic (EM) circuit co-optimization approach based on an electromagnetic database (EMDB). This study is the result of long-standing efforts toward the development of an efficient planar EM simulator and its seamless integration in and combination with a circuit design environment. Two complementary techniques are put forward to build an EMDB model. Flexibility, accuracy, and computational efficiency of both techniques are validated by several examples.**

***Index Terms*—Circuits, co-optimization, electromagnetic database (EMDB), method of moments (MoM).**

I. Introduction

WHEN designing RF, microwave, and millimeter-wave circuits (and this designation also includes the broadest possible range of circuits from multigigabit/s digital boards and packages to waveguide filters, multiplexers, antennas, etc.), it is generally accepted that optimization within reasonable CPU time limits should be based on conventional circuit-oriented simulators. These simulators use the description of a circuit in terms of lumped elements and (coupled) transmission lines to account for distributed effects and/or directly rely on an S-parameter (or, equivalently, Y or Z-parameter) description of the different parts of the circuit. All of this is well known and we will not go into detail here. The circuit simulator approach in general relies on a divide-and-conquer technique in which the circuit is subdivided into separate parts for which models exist or can be calculated (either semianalytically or using a dedicated electronic design automation (EDA) tool). Kirchoff's current and/or voltage laws are then applied to obtain the overall circuit equations and solutions.

The advantages of the circuit simulator approach are clear: this approach is fast and, therefore, easily integrated with advanced optimization techniques. Moreover, the circuit partitioning appeals directly to the designer. However, the partitioning and circuit description, which go hand in hand, do not always properly account for the actual field effects that occur in the circuit. To properly design microwave, RF, and high-speed digital circuits, it is necessary to take into account the physical effects of the actual physical layout. Powerful electromagnetic (EM) solvers have emerged to predict these effects, which are often described as parasitic effects. When considering the more general class of microwave and millimeter-wave circuits [(waveguide) filters, multiplexers, antennas, etc.], it becomes even less evident to make the distinction between the circuit description and EM behavior, as physical effects here are often an integrated part of the desired circuit behavior.

From the above reasoning, it would seem natural to rely more heavily on EM solvers for circuit design and optimization purposes. However, this is hampered by at least two drawbacks. Although in the past decade much progress has been seen in the development of efficient field solvers, accompanied by a very large increase in computer speed and memory, field solvers ultimately remain slow with respect to circuit solvers. This lack of speed is especially detrimental for optimization, tuning, yield analysis, etc., which require a large number of circuit evaluations. Secondly, EM solvers are suited for the passive linear part of the circuit, but it is much more difficult to include active and nonlinear elements, which can more easily be incorporated in circuit analysis.

Referring to Fig. 1, the EM/circuit analysis and optimization problem can be viewed as follows. EM field simulators offer highly accurate results, but this accuracy most often comes with slow performance in terms of CPU time and high memory requirements. On the other hand, conventional circuit simulators are somewhere in the lower right corner of this figure. They are fast and highly flexible, but do not account for all field effects, and accuracy strongly depends on the available models and is not always guaranteed. Hence, the question arises as how to

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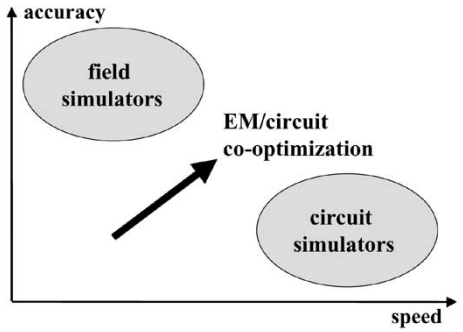

Fig. 1. Field-circuit optimization problem: a global perspective.

properly combine field analysis and circuit analysis in such a way that the respective advantages yield a new type of EDA tool that can be positioned somewhere in between EM and circuit tools, as indicated by the arrow in Fig. 1.

It is certainly not our purpose here to discuss the various types of EM (or circuit) simulators and their advantages and disadvantages. Several authors of this paper have been involved for a long time in the development of a method of moments (MoM) computer-aided design (CAD) tool for planar type of circuits. Recent advances make it possible to analyze complex digital circuits with a large number of ports [1]. Hence, in the sequel, we will focus on EM/circuit co-optimization relying on the MoM analysis of the problem. It will, however, become clear that the discussed techniques remain valid when replacing the MoM solver by another EM CAD tool, e.g., based on a finite-element or finite-difference time-domain (FDTD) solution of Maxwell's equations.

The remaining part of this section is devoted to a brief overview of the literature on the combination of EM and circuit analysis for optimization purposes. Over the past decade, this literature is very abundant and we will mainly restrict ourselves to those papers that are the most relevant in the context of the research efforts presented in the sequel.

An early contribution to the combination of field and circuit analysis is to be found in [2]. Here, a time-domain simulator based on the spatial network method (SNW) (a method closely related to the transmission-line matrix (TLM) method) is used, for example, to combine a coplanar transmission line with several Schottky varactor diodes. This paper already emphasizes the fact that nonlinear elements are to be included through their circuit equivalent, but should be combined with EM analysis to properly account for all distributed effects. It is also interesting to remark that the author concludes that "the need for large computer power limits the practical use of this method," a conclusion which remains partly valid, even today, be it that much larger and complex geometries can be handled by EM solvers. The need for advanced physics-oriented models of active circuits was also recognized early. We refer the reader to [3] for a thorough treatment of this topic and to the impressive literature overview provided by this paper.

Some problem classes lend themselves quite naturally to a two-step procedure in which the circuit is first partitioned, followed by a field analysis whereby each part is characterized at its ports by S-parameters. This approach is particularly successful in the modeling of waveguide devices such as beam-forming networks and phase shifters, e.g., as in [4] and [5], where mode-matching techniques are used as the preferred field analysis technique. For an overview of recent advances and CAD-tool capabilities in this domain, we also refer the interested reader to the workshop contribution of Arndt in [6] and Arndt *et al.* in [7].

In [8], the need to combine circuit analysis and full-wave models is also emphasized. Initial design of a manifold multiplexer is performed using simple circuit analysis. In a subsequent step, the manifold is rigorously described by a full-wave model, while the filter elements are still modeled by a circuit approach and, finally, the entire structure is optimized in a full-wave way. This clearly shows the power of circuit/EM co-simulation and optimization and draws attention to the important fact that the weight attributed to either the circuit approach or the EM approach will typically vary over the different design stages.

Pioneering work in the use of direct EM optimization, allowing to reach the design specifications with full EM accuracy by automatically adjusting physical layout parameters, is presented in [9]. The most often prohibitive amount of CPU time needed for direct EM optimization led Bandler *et al.* to the development of the space mapping (SM) [10] and aggressive SM [11] techniques. In the (aggressive) SM technique, the behavior of a system is described in two spaces: the optimization space (OS) and the electromagnetic space (EMS) (also indicated as the validation space). The OS space can be comprised of empirical models or of an efficient coarse grid EM space. To make clear what this means, we cite one of the examples treated in [10], where a double-folded stub filter is optimized in an OS constituted by course grid EM simulations, i.e., EM simulations with a grid of 4.8 mil $\times$ 4.8 mil surface current discretization cells. The EMS or validation space is constituted by fine-grid EM simulations, i.e., EM simulations with a grid of 1.6 mil $\times$ 1.6 mil surface current discretization cells. The purpose of this approach is clear: the number of costly EM simulations should be kept as low as possible and this cost drastically increases when using a finer grid. On the other hand, too coarse a grid could lead to incorrect results. In the (aggressive) SM technique, a transformation mapping the fine model parameter space to the coarse model parameter space (and vice versa) is constructed and misalignment of responses in both spaces as a function of frequency is alleviated by introducing frequency SM. The SM technique clearly points the way toward an intermediate level needed between EM space in its full detail and the circuit modeling level pure and simple. Very recently, a further refinement of the SM concept was presented in [12].

In [13], the well-known partial-element-equivalent-circuit (PEEC) technique is put forward to hierarchically model interconnect networks. As PEEC leads to a SPICE network representation of the interconnection, this network representation can then easily be incorporated in an overall circuit analysis. This avoids the intermediate level used in the SM technique, but suffers from the fact that PEEC networks can become very large and will obviously also require a lot of CPU time when the geometrical parameters change while optimizing a circuit. A somewhat related approach, i.e., creating a circuit equivalent from EM data, is presented in [14]. Here, the FDTD method is used in conjunction with an equivalent circuit model for a silicon on plastic (SOP) electronic package. References [15]

and [16] are representative of many other contributions that can be found in literature in which EM data are used to project onto a circuit model (which could typically combine lumped elements with transmission lines). An interesting more recent example is provided by [17].

At this point, we would already like to make clear that we initially also tried to pursue this path [18] when trying to use EM data from a planar MoM solver in an efficient way. It soon became clear, however, that this was hampered by several disadvantages. The first problem is the availability of a suitable circuit model. If one wants to handle a large class of RF and microwave circuits, existing circuit model topologies might be either quite inaccurate or even lacking. Moreover, it turns out to be quite difficult to find topologies that are sufficiently broad-band, while presenting the user with different topologies for different frequency bands is highly undesirable. Finally, lumped-element values derived from EM analysis turn out to be quite sensitive to the parameters that control the EM simulation, in particular, the size of the mesh cells.

To conclude this section, it should, of course, be made clear that present-day commercial EM solvers offer direct EM optimization possibilities in which many of the existing optimization approaches can directly be applied to the EM results. In that case, the EM solver is simply part of a classical optimization loop. We will also come back to this direct optimization approach at the beginning of Section II.

The speed of the optimization process critically depends upon the time needed to solve the EM problem and this can quickly become problematic. Optimization efficiency can greatly be enhanced when gradients are available. One way to extract this gradient information is to use two or more simulation results to approximate the gradient by taking finite differences. This involves several repeated analyses of slightly perturbed problems. This approach is error prone for two reasons: numerical error in general and the fact that changes in the meshing that come with small changes in, e.g., the geometrical parameters of the problem, can have a very detrimental effect on the final results. Furthermore, the cost in terms of the number EM analyses is high. This drawback can, however, be removed by using analytical approaches to directly obtain gradient information from a single EM analysis. The finite-element method (FEM) is known to provide such gradient information at little extra cost [19]. Recent contributions to FEM-based optimization can be found in [20] and [21], while [22] combines gradient-based optimization with an FDTD field solver.

We have demonstrated in the past [23] that MoM solvers also lend themselves to the calculation of analytical gradient information from a single EM analysis. This comes with a limited cost as the so-called system interaction or Z-matrix can be reused with a different excitation or source vector (the calculation of which requires additional CPU time). A new adjoint sensitivity technique in combination with a MoM EM solver has recently been proposed in [24].

In the new circuit/co-optimization approach presented here and in [25] and [26], gradient information can also be obtained, but this information is still extracted using finite differences. However, special care is taken to minimize the number of EM analyses and to circumvent the mesh-related noise problems associated with the analysis of slightly perturbed geometries.

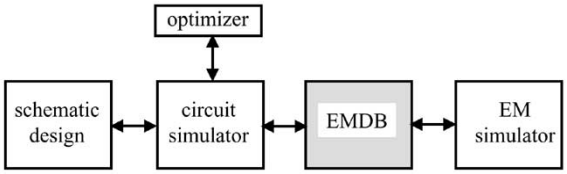

Fig. 2. Block diagram of the EM-circuit co-optimization environment showing the EMDB.

The above short overview of different optimization approaches is by no means complete. In recent years, genetic algorithms (see [27] and [28] among many others) have been put forward as a versatile means to optimize complex structures. In [29] a [two-dimensional (2-D)] space and time-adaptive multiresolution time-domain (MRTD) algorithm is promoted as an efficient EM method to be combined with optimization, while in [30], the TLM method is used in an original way to directly optimize microwave topologies.

It is by now quite clear that EM-based optimization is a rich, complex, and evolving research topic of great practical interest and we would like to turn to our own contribution.

This paper is further organized as follows. In Section II, we present a new approach that is the ultimate outcome of our ongoing research toward the efficient combination of EM and circuit analysis. Both the general layout component (GLC) and the electromagnetic model database (EMDB) concept are introduced. Section III discusses a first on-the-fly type of technique to generate a GLC–EMDB model for a circuit. Section IV discusses a second up-front type of technique to generate such a model. Each technique is illustrated by a number of examples. Finally, some concluding remarks are formulated in Section V.

II. Model Database Approach for EM/Circuit Co-Optimization

A. General Block Diagram of the Optimization Process

From Section I, two approaches to the EM-circuit optimization problem emerge. A first approach is the direct one, in which the EM solver is driven directly within a classical optimization loop. We already mentioned the pioneering work of [9], soon followed by [31]. In [31], EM optimization and nonlinear harmonic-balance simulation are integrated, enabling to combine physical layout optimization with optimization of the nonlinear circuit performance. The second approach is the indirect one, where a suitable intermediate level is used between the EM results and the circuit design environment. Lumped elements (including (coupled) transmission lines) are often used, but it was again Bandler *et al.* [10], [11] who clearly expressed the need for the generalization of this intermediate level by introducing the (aggressive) SM technique.

Drawing upon previous experience and aware of the fact that the direct approach will always suffer from the inherent speed limitations of EM solvers (most certainly so when taking into account the need of the designer to analyze ever more complex often multiport circuits), we have developed an indirect approach whereby an EMDB is constructed and used as the intermediate level between the EM solver and the circuit simulator design environment. Fig. 2 shows a block diagram of the

complete design environment. As can be seen, the optimization is performed by the circuit simulator, as such preserving the full flexibility to combine transient time- or frequency-domain analysis (dc, ac, harmonic balance, envelope analysis, ...) with EM generated models. In this approach, the circuit optimization process, i.e., the realization of specific design goals, has the full flexibility to allow for simultaneous variation of the lumped-component values and of the physical-layout parameters. To introduce these physical-layout parameters into the optimization process in a way that is completely transparent to the circuit simulator and, hence, to the designer, the notion of GLC was first introduced in [25]. In a schematic circuit design environment, we are very familiar with the usual symbolic representation of lumped elements (resistors, capacitors, inductors, ...), coupled transmission lines, and active elements. The GLC feature extends the list of schematic circuit element representations with an unlimited number of additional representations automatically derived from the physical layout of a particular planar circuit. To clarify the GLC concept, we will immediately turn to an example in Section II-B, but let us first complete the further explanation of the block diagram of Fig. 2. When the circuit simulation engine encounters a GLC in the netlist of the circuit under investigation, it will check if a model for this GLC is available in the EMDB. This model is an S-parameter model. When missing, the EM solver will be invoked to gather the necessary data to construct the model of the GLC in the EMDB. It is very important to already emphasize at this point that the designer has several options at his disposal to construct such models, ranging from the *a priori* construction of a set of models in the EMDB to an on-the-fly construction of such a model while the optimization process is taking place. As EM simulations are very costly, care is taken to limit the number of simulations as much as possible and to select the parameters of each EM simulation such that maximal extra knowledge about the GLC is obtained with each additional EM simulation. How this is achieved is discussed in Sections III and IV.

As remarked by two of the reviewers, the possibility of using an artificial neural network (ANN) could be considered. However, the difficulty to determine the proper topology of such a network together with the fact that a long training process is necessary, which requires many data points (which is precisely what we seek to avoid), has driven our research to construct a model database into another direction.

B. GLC

Further details about the GLC concept can best be explained by means of an example. To this end, we have selected the analysis and optimization of the low-noise amplifier (LNA) depicted in Fig. 3. Fig. 3 shows the schematic design of the amplifier circuit. The active element is a double emitter bipolar junction transistor for which a Gummel–Poon npn model is available. The schematic also shows a number of lumped resistors and capacitors. Accurate analysis and optimization of this amplifier is impossible without taking into account the RF board on which the active and passive components will be mounted. Fig. 4 shows the footprint of this RF board. To make it easy for the designer to connect the lumped elements with the footprint of the RF board

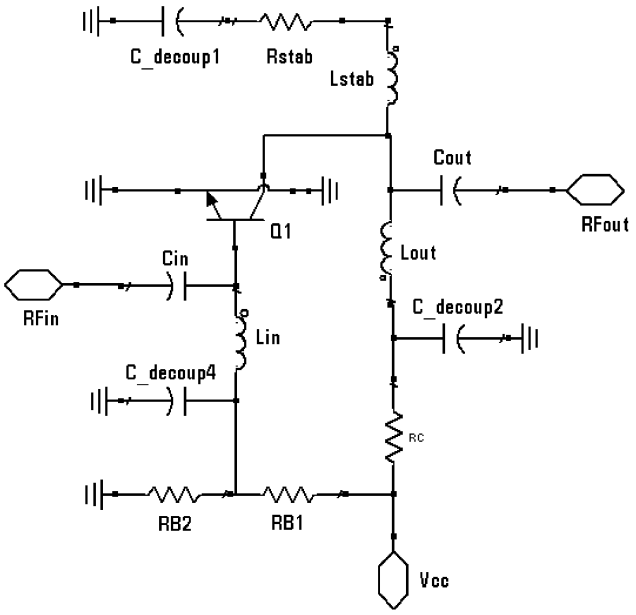

Fig. 3. Schematics of an LNA.

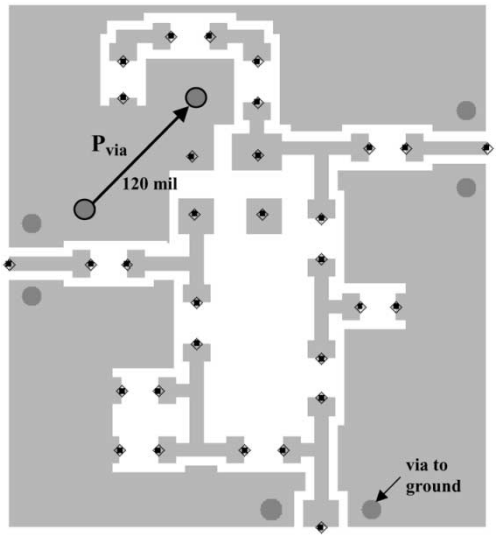

Fig. 4. Footprint of the RF board layout for the LNA of Fig. 3.

in the schematic design, a layout look-alike schematic symbol for the GLC component, representing the RF board footprint, is automatically created. The pins of this symbol correspond with the physical location of the ports in the layout. Placing this symbol in the schematic design environment and connecting all the lumped elements to the corresponding pins of the GLC component yields a new schematic representation of the amplifier circuit, but now with the actual layout parasitics included (see Fig. 5). Of course, creating the layout look-alike symbol does not suffice. The definition of the GLC is completed with the following two sets of parameters to be added by the user.

- *Simulation control parameters*: these parameters define the setup of the EM simulations during the S-parameter calculations needed to create or extend the EMDB model of the GLC. Typical parameters are the mesh settings and frequency range.

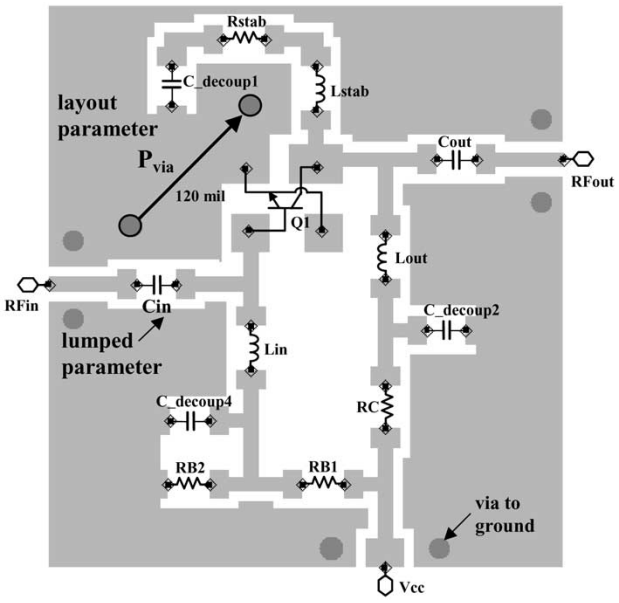

Fig. 5. Schematic of the LNA including the GLC for the RF board footprint, as depicted in Fig. 4.

- *Layout parameters*: these parameters can vary in a continuous way and will do so when going through the optimization process. In the LNA example, a single layout parameter will be introduced, i.e., the position of one of the grounding vias (the grounding via of the emitter contact). The position of this grounding via will be varied along the full line shown in Figs. 4 and 5 to assess the influence of its parasitic effect.

The lumped elements themselves are treated in the usual way and can be subjected to an optimization process in conjunction with the layout parameters of the GLC. This will be illustrated in Section III by considering the joint optimization of the via-hole position and the value of the lumped input capacitor C_{in}.

C. EMDB

The EM solver used in our study is based on the MoM solution of a frequency-domain mixed-potential integral equation [32] for the currents and charges on the metallizations and vias or for their magnetic counterparts when slot circuits are considered. Typical output data are the S-parameters at the ports and the current distribution. As explained in Section I, previous research efforts have revealed that the S-parameter data themselves were better suited than equivalent-circuit models or pole-zero models to build an EM database model for a particular circuit, most certainly so when a multidimensional parameter space has to be covered and this over a broad frequency range. Two techniques were developed to build the EMDB. The on-the-fly-oriented technique is discussed in Section III, while the up-front one is treated in Section IV. It should be mentioned that at present the on-the-fly approach has been fully integrated within a commercial EDA tool,[1] while the second, i.e., the up-front approach, is also available to the user, but as a separate module.[2] It is clear that both approaches are complementary and the user will further benefit by their future integration.

III. Minimal-Order Multidimensional Linear Interpolation Technique

A first possibility is to use the highly dynamic interpolation scheme as first reported in [26]. In this case, the circuit simulator first determines if a model for the GLC is already available in the EMDB. If not, a minimal number of EM simulations are initiated as required by the build-in multidimensional and minimal-order linear interpolation scheme. In this approach, the EMDB associated with the GLC decides if the required new data point during the circuit optimization can safely be derived from existing data (through interpolation) or if new data points (and, hence, new EM simulations) are needed. The number of new data points is minimized in order to drastically restrict the number of costly EM simulations. It is clear that once a sufficient number of data points has been collected and stored in the EMDB, most of the new data points requested by the optimizer will be available through interpolation, which yields a much faster result than an actual EM simulation. The number of EM simulations needed to complete the optimization process is strongly problem dependent. Let us now take a closer look at the interpolation scheme.

Consider a GLC with N layout parameters $(p_1, p_2, \ldots, p_N)$, which are allowed to vary during the optimization process. The term "data point," as used in the above description, corresponds with a particular set of values for these N parameters and is denoted by the vector $\mathbf{P}^i$ in N-dimensional space, where the superscript i relates to the ith datapoint. Suppose a set of $(M+1)$ data points $\{\mathbf{P}^0, \mathbf{P}^1, \ldots, \mathbf{P}^M\}$ with $1 \leq M \leq N$ has already been generated. Provided the set of M difference vectors $\{\mathbf{P}^0 - \mathbf{P}^1, \ldots, \mathbf{P}^0 - \mathbf{P}^M\}$ is linearly independent, this set spans an M-dimensional subspace in the N-dimensional parameter space. In this subspace, each data point $\mathbf{P}$ can be represented by its M subspace coordinates as

$$\mathbf{P} = \sum_{j=0}^{M} \mathbf{r}_j \mathbf{P}^j \tag{1}$$

with the extra coordinate r_0 defined as

$$\mathbf{r}_0 = 1 - \sum_{j=1}^{M} \mathbf{r}_j. \tag{2}$$

The S-parameter data in data point $\mathbf{P}$ are obtained by M-dimensional linear interpolation through

$$S(\mathbf{P}) = \sum_{j=0}^{M} \mathbf{r}_j \, S\big(\mathbf{P}^j\big). \tag{3}$$

This approximation will only be good if the new data point falls inside the volume generated by the original set

[1] *Momentum EEsof EDA*, Agilent Technol., Santa Rosa, CA.

[2] *Advanced Model Composer EEsof EDA*, Agilent Technol., Santa Rosa, CA.

$\{\mathbf{P}^0, \mathbf{P}^1, \ldots, \mathbf{P}^M\}$, i.e., no "dangerous" extrapolation is allowed. This will be the case provided:

$$0 \leq \mathbf{r}_j \leq 1. \tag{4}$$

Furthermore, data point $\mathbf{P}$ must be "sufficiently close" to the original set. Here, a distance measure is needed. We use the L_1 distance defined by

$$L_1(\mathbf{P}, \mathbf{P}^j) = \sum_{k=1}^{N} \left| \frac{p_k - p_k^j}{\Delta p_k} \right| \tag{5}$$

where the weighing factor Δp_k for each layout parameter p_k is determined by the user. In our implementation, "sufficiently close" corresponds with $L_1 < N$ with N being the number of layout parameters. For geometrical parameters, the user is advised to select a Δp_k given by $0.01 * \lambda_{\text{free-space}}(f_{\max})$/(mesh density), where the mesh density corresponds to the number of mesh cells per wavelength and $f_{\max}$ is the highest frequency considered in the simulations. This guideline for choosing Δp_k makes sure that variations of p_k when performing a series of EM simulations remain small enough to avoid that changes in the behavior of the circuit would become too large as a consequence of abrupt changes in the electrical length of the considered parameter. At the same time, this cautious choice of Δp_k assures that trustworthy gradient information will become available (see also a further remark on gradient information at the end of this section).

To minimize the number of EM simulations, the following remark is of crucial importance. When a new data point $\mathbf{P}$ is requested by the optimizer, it is certainly not always necessary to use all the data points that are already available to invoke the interpolation procedure (3). Indeed, the first action is to look for the minimal M and corresponding $M+1$ linear independent sample points that are already available and that satisfy the condition $L_1(\mathbf{P}, \mathbf{P}^j) \leq N$ together with requirement (4). Although this sounds quite complicated, it amounts to saying that, e.g., for a 2-D parameter space $(N = 2)$, interpolation over a line segment $(M = 1)$ will first be considered before interpolation over a triangle $(M = 2)$. If no value of M satisfying all requirements is found, new EM simulations become necessary. The available set of data points is scanned for an existing data point $\mathbf{P}^k$, which shares the largest number of layout parameter values with the new data point $\mathbf{P}$. The value of M is now selected to be equal to the number of layout parameters that are distinct for $\mathbf{P}$ and $\mathbf{P}^k$, and M EM field calculations are performed in a suitably selected neighborhood of $\mathbf{P}^k$. Using these new EM results, the S-parameters for data point $\mathbf{P}$ are again found by using (3).

Let us first take a look at a simple test case. Fig. 6 shows the layout of a four-turn octagonal spiral inductor on a silicon substrate with linewidth of 15 μm and a separation between the windings of 5 μm. Surrounding the inductor is a metallization ring that acts as the patch for the return current in the structure. This metallization ring is also connected to the silicon substrate using a number a square-shaped vias. The area occupied by the spiral inductor is controlled by the layout parameter W, which is the radius of the inner winding. Fig. 6(a) and (b) shows the layout of the spiral inductor for $W = 45$ μm and $W = 85$ μm, respectively. The silicon substrate has a thickness of 500 μm

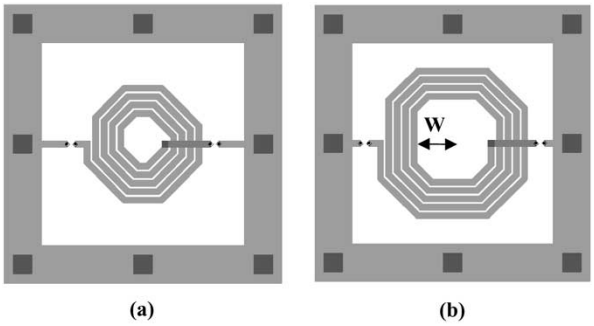

Fig. 6. Layout of a four-turn octagonal silicon spiral inductor. (a) $W = 45$ μm. (b) $W = 85$ μm.

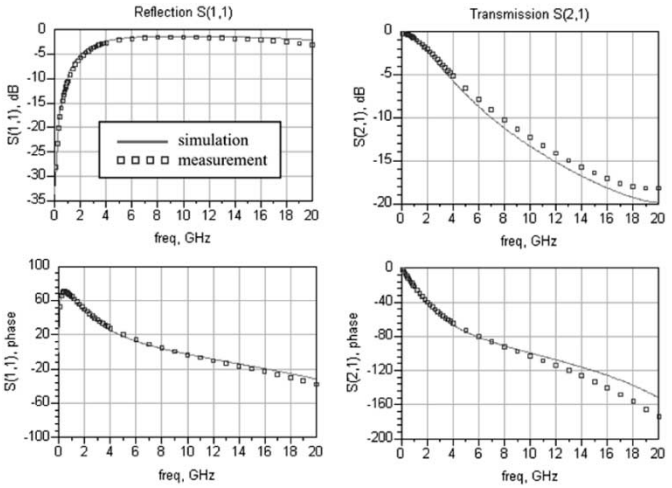

Fig. 7. Simulated and measured two-port S-parameter data for the spiral inductor with $W = 65$ μm.

and a resistivity of 15 $\Omega \cdot$ cm. The SiO_2 layer on top of the silicon substrate has a thickness of 8 μm. The simulation results obtained with the planar EM engine are first validated by comparing the simulated two-port S-parameters with measured data available for $W = 65$ μm. To this purpose, a layout component was created for the spiral inductor. During the circuit S-parameter simulation, the EM engine is automatically invoked and the resulting inductor model is stored in the EM database associated with the layout component. Fig. 7 shows the two-port S-parameters from the EM engine together with the measured data. Excellent agreement is seen in the entire frequency band. The wide-band simulation (0–20 GHz) performed with MomentumRF took approximately 3 min of CPU time on an HP B2000 Unix Workstation, requiring less than 6 MB of RAM. The mesh used in the simulations counted 20 cells per wavelength and an edge mesh was introduced to enhance the accuracy.

EM simulations or measurements yield S-parameter data, which can be used directly as a model for the spiral inductor in subsequent design steps. However, it is more convenient and useful for design purposes to use a number of derived quantities. For the spiral inductor, the most important ones are the inductance value and quality factor. To obtain these quantities, the reflection coefficient seen at the first port is simulated with the other port shorted. From this, the inductance value L and the quality factor Q for the spiral inductor are easily calculated from $R + j\omega L = 50(1 + S_{11})/(1 - S_{11})$

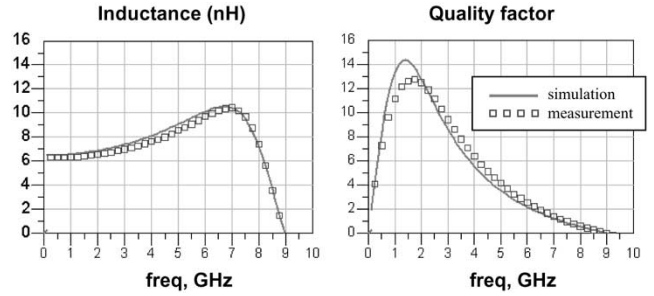

Fig. 8. Simulated and measured inductance value and quality factor for the spiral inductor with $W = 65$ μm.

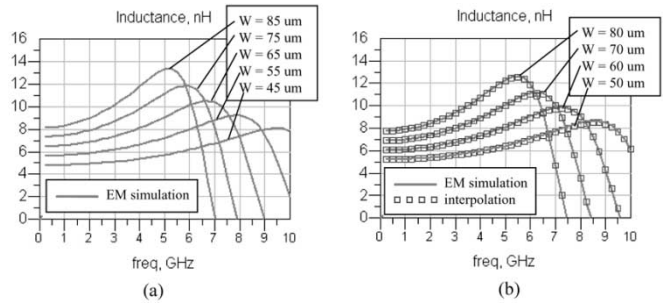

Fig. 9. (a) Simulated inductance for different values of the layout parameter. (b) Interpolated inductance for intermediate values of the layout parameter.

and $Q = \omega L/R$. The resulting plots for the EM simulated and measured values for L and Q as a function of the frequency are shown in Fig. 8 (again for $W = 65$ μm). During the circuit S-parameter simulation, the model for the spiral inductor is retrieved from the EM database associated with the layout component. The values for L and Q determined from the measured and simulated data correspond well. Note that, above 9 GHz, the frequency-dependent inductance value becomes negative as does the quality factor, indicating that capacitive effects are dominating the behavior of the spiral at these frequencies.

In order to verify the interpolation-based models in the EM database, the inductance of the spiral was simulated for five different values of the layout parameter ($W = 45, 55, 65, 75, 85$ μm), each simulation taking up approximately 3 min of CPU time. The resulting plots are displayed in Fig. 9(a). Next, the inductance values for the intermediate parameter values ($W = 50, 60, 70, 80$ μm) have been obtained using the interpolation scheme. The interpolated results are compared to the values obtained from direct EM simulation in Fig. 9(b). To highlight the computational efficiency of the interpolation-based modeling, we note that, for each additional simulation, the CPU time using the EM-database interpolated models was less than 2 s, as compared to a few minutes for the EM simulation. This is a significant gain in speed, which, in combination with the relatively small error, provides an efficient and powerful modeling approach for real-time tuning and optimization of circuit layout parameters.

We now turn again to the LNA example of Fig. 3. Its gain was simulated using the circuit simulator from the Advanced Design System (ADS) software from Agilent Technol., Santa Rosa, CA. Fig. 10 shows the results of the original schematic up to 2 GHz [result 1 (o)]. The gain reaches a peak of 19 dB at approximately 0.5 GHz. This simulation does *not* include the parasitics from

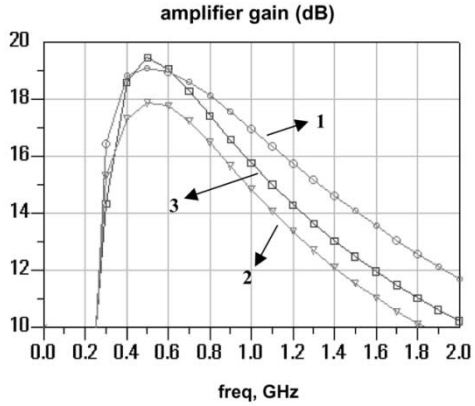

Fig. 10. Amplifier gain as a function of frequency for the amplifier of Fig. 3 (1: original schematic (O), 2: result including board parasitics (∇), 3: result after optimization ($\square$)).

the board (pure lumped-element simulation). When including these parasitics by applying the procedure described above (i.e., using the GLC–EMDB model of the amplifier), the amplifier gain drops by approximately 1 dB (result 2 (∇) on Fig. 10).

In order to further optimize the design, two design parameters are introduced. The first one, i.e., p_1, is the value of the input capacitor C_{in} (see Fig. 3). The second one, i.e., p_2, is the position P_{via} of the via-hole along the line shown on Figs. 4 and 5. Their initial values (i.e., the values already used in the above simulations) are $C_{\text{in}} = 12$ pF and $P_{\text{via}} = 20$ mil. The trajectory that can be covered by the via is indicated in Figs. 4 and 5 by displaying both the beginning and end positions of that trajectory (denoted by the shaded circles in Figs. 4 and 5. The optimization goal is to maximize the amplifier gain between 0.4–0.6 GHz. The gradient-based optimization stopped after 13 iterations, requiring a total of 11 EM simulations with MomentumRF, each taking up approximately 2.5 min of CPU time on an HP Kayak XA Pentium II 330-MHz computer (again using 20 cells per wavelength and an edge mesh). The resulting gain curve is also displayed in Fig. 10 [result ($\square$)], showing an improvement of almost 2 dB over the nonoptimized result. The optimum parameter values are $C_{\text{in}} = 120$ pF and $P_{\text{via}} = 89.73$ mil. Note that the position of the via in the optimized design is as close as possible to the emitter contact.

To complete this discussion, a final remark should be made. The optimization process can very much benefit from the availability of gradient information. As explained in Section I, gradient information obtained by finite differences from EM simulations with (very) small variations in the parameter values are error prone. In the above interpolation scheme, however, gradient information is always obtained through linear interpolation in a set of data points separated by a large enough distance. This makes the gradient information very trustworthy.

IV. Multidimensional Adaptive Parameter Sampling Technique

Let us now turn to a second technique, which can be adopted to construct an EMDB-model. This approach does not aim at the dynamic on-the-fly type of use of EM simulation data, but is rather intended as being used up-front. As in the previous

technique, the purpose remains to construct an S-parameter data model. However, this model is not constructed under the direct command of the optimizer, but the modeling task is reformulated as follows. The N-dimensional layout parameter space is defined by the user by specifying the range of values that can be taken by each parameter p_k, i.e., $p_{k,\min} \leq p_k \leq p_{k,\max}$. This is also the case for the frequency range, i.e., $f_{\min} \leq f \leq f_{\max}$. The question is now the following: how can a model for the S-parameters be constructed with a predefined error limit over the whole parameter space and the whole frequency range and this with a minimal number of data points, i.e., with a minimal number of EM simulations? Once such an up-front model is available, it is clear that it can directly be used in an optimization process, provided we keep within the boundaries of the predefined parameter space and frequency range. Moreover, as the model is valid for the whole parameter space, gradient information will again be trustworthy.

To obtain such an up-front model, we developed the so-called multidimensional adaptive parameter sampling (MAPS) technique first reported in [33]. We will not go into much detail here, but restrict ourselves to the salient features of the technique as compared to the technique discussed in Section III.

The S-parameter data are now represented as

$$S(f,\mathbf{P}) = \sum_m C_m(f)\, F_m(\mathbf{P}). \tag{6}$$

In (6), an S-parameter is written as the weighted sum of the orthonormal multidimensional polynomials F_m. These multinomials only depend upon the layout parameter vector $\mathbf{P}$, which is identical to the vector used above in (1), (2), (3), and (5). The frequency dependence of the S-parameters is introduced via the weights C_m. These weights can be calculated by fitting a set of Q data points $\mathbf{P}^s$, with s ranging from 1 to Q. Detailed information about the polynomials F_m and their construction can be found in [33]. Orthogonality of the polynomials means that the following relationships hold:

$$\sum_{s=1}^{Q} F_k(\mathbf{P}^s)F_k(\mathbf{P}^s) = \delta_{kl} \tag{7}$$

with δ_{kl} being the Kronecker delta. The weights C_m satisfy

$$C_m(f) = \sum_{s=1}^{Q} \mathbf{S}(f,\mathbf{P}^s)F_m(\mathbf{P}^s). \tag{8}$$

For a single layout parameter p_1, (6) reduces to a polynomial in p_1. The highest power will be $(p_1)^{Q-1}$. When there are two or more layout parameters, the F_m's will be products of powers of the parameters, e.g., $(p_1)^1(p_2)^3(p_3)^1 \ldots$ The following questions still have to be answered.

i) How does one select the data points $\mathbf{P}^s$ in such a way that a minimum number of data points and, hence, a minimum number of EM simulations suffices?

ii) How does one choose the F_m's, i.e., which multinomials have to be included in (6) and which powers of the parameters to use?

iii) How does one model the frequency dependence (remark that in (8) the frequency is still a continuous parameter)?

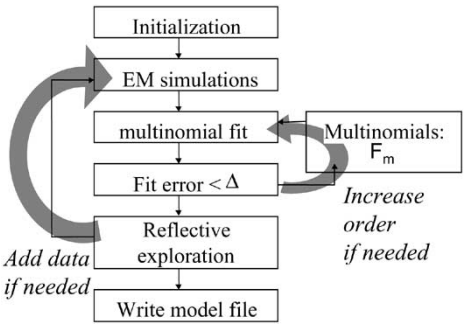

Fig. 11. Flowchart of the up-front generation of a MAPS–EMDB model of a generalized layout component.

The adaptive process used to select data points and to construct the model is based on nonstatistical reflective data exploration [34]. This method is particularly useful when the cost of obtaining a data point is high, as in our case. To apply the method, a reflective function is needed. The following reflective function is introduced:

$$\begin{aligned} R(f,\mathbf{P}) &= \left| \sum_{m=1}^{M_{\text{new}}} C_m(f)F_m(\mathbf{P}) - \sum_{m=1}^{M_{\text{old}}} C_m(f)F_m(\mathbf{P}) \right| \\ &= \left| \sum_{m=1+M_{\text{old}}}^{M_{\text{new}}} C_m(f)F_m(\mathbf{P}) \right|. \end{aligned} \tag{9}$$

$R(f,\mathbf{P})$ is the absolute value of the difference between the previous model built with M_{old} multinomials and the new one built with M_{new} multinomials. New data points are selected in the neighborhood of the maxima of $R(f,\mathbf{P})$ over the whole parameter space until $R(f,\mathbf{P})$ drops below a prescribed error limit Δ (e.g., -60 dB). Furthermore, additional reflective functions are introduced. For passive circuits, we have that $|S_{ij}| \leq 1$. If these passivity requirements are violated, new data points are introduced where these requirements are violated the most. If a scattering parameter exhibits local minima or maxima, modeling accuracy requires data points near these extremes. If this is not yet the case in the model, data points are introduced at the extrema of the model. Finally, the power loss at a port will show a local maximum at a resonant frequency. These maxima are also selected as the preferred data points. Further details are given in [33], but the whole process can be summarized by the flowchart displayed in Fig. 11.

With regard to the second and third questions, we will be brief here. The selection of the F_m's starts from a series of one-dimensional analyses whereby one layout parameter, say, p_i, is allowed to change, while the others, i.e., $p_j (j \neq 1)$, are kept constant at their midpoint value. The more important the influence of p_i on the GLC model, the higher the order of the polynomials needed to obtain a sufficiently accurate one-dimensional fit will be. The maximum order for each parameter is then used as a reference to assign a relative importance to each parameter while applying the reflective exploration procedure, more in particular when deciding which specific multinomials $F_m = (p_1)^i(p_2)^j(p_3)^k, \ldots,$ to include. Details can again be found in [33]. As to the frequency dependence, a number of discrete frequencies f_j, $j = 1, 2, \ldots; N_f$ is first selected through the adaptive frequency sampling algorithm described in [35].

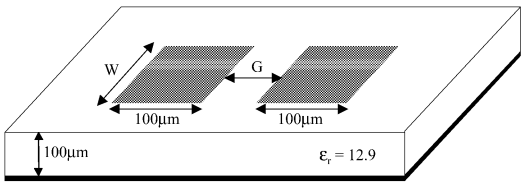

Fig. 12. Microstrip gap on a GaAs substrate.

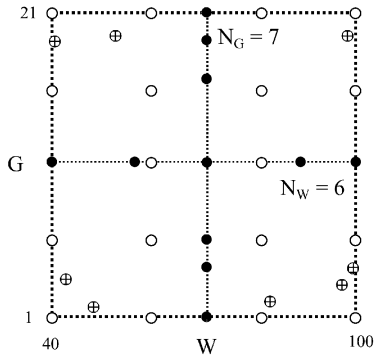

Fig. 13. Adaptive data point distribution for the microstrip gap of Fig. 12.

The MAPS technique is then applied at each frequency f_j. This will, in general, result in a model (6) with a different number of F_m's for each frequency. In a last step, an overall model is constructed based on the maximum number of multinomials F_m encountered over the whole frequency range.

We illustrate the MAPS approach with three examples. The first example is that of the microstrip gap on a 100-μm GaAs substrate, shown in Fig. 12. The layout parameters are $p_1 = W$ with 40 μm $\leq W \leq$ 100 μm and $p_2 = G$ with 1 μm $\leq W \leq$ 21 μm. The frequency ranges between dc and 60 GHz. This example is also treated in [33] (where S-parameter data as obtained with the MAP's approach and with a series of straightforward EM simulations are shown to agree completely). Here, we only want to draw attention to the adaptive data point selection, as shown in Fig. 13. As explained above, two one-dimensional analyses are first performed: a first one for $G = 11$ μm with W varying from 40 to 100 μm and a second one for $W = 70$ μm with G varying from 1 to 21 μm. The first analysis required six data points (the black dots in this figure) and four F_m functions. The second one required seven data points and six F_m functions. The prescribed error limit Δ is -60 dB, i.e., $|R(f, \mathbf{P})| \leq -60$ dB. As a consequence of these one-dimensional analyses and when further expanding the model in the whole (G, W)-plane, more importance will be attached to powers of G than to powers of W. In a first reflective expansion of the model, a new set of data points is selected, as indicated by the nonfilled dots in Fig. 13 (12 in total). A second expansion of the model is needed to reach the required final accuracy. The data points corresponding with this second iteration (eight in total) are the dots with crosses in this figure, leading to a grand total of 32 data points and, hence, EM simulations. The expansion (6) used in the final model (both for S_{11} and S_{12}) is

$$S(f,W,G) = \sum_{i=0}^{5}\sum_{j=0}^{3} C_{ij}(f) G^i W^j + C_{04}(f) W^4 + C_{14}(f) G W^4 + C_{60}(f) G^6 \quad (10)$$

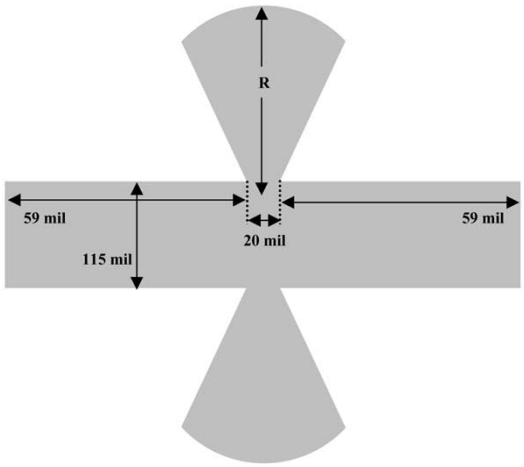

Fig. 14. Top view of the layout of a butterfly capacitor.

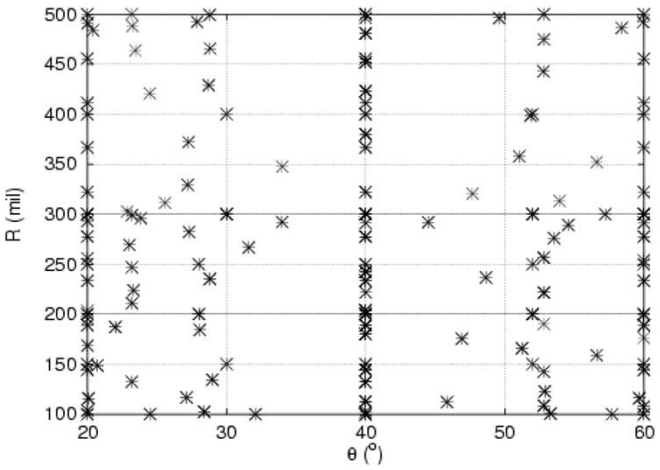

Fig. 15. Adaptive data point distribution for the butterfly capacitor of Fig. 14.

i.e., 27 multinomials in total, with a clear dominance of the powers of G. We have carefully checked the resulting S-parameter accuracy with respect to full-wave simulations in 1077 test structures in 51 frequency points and the overall error level turned out to be -56 dB. That the desired -60 dB could not be obtained is due to the inherent noise level of the EM calculations.

The second example is that of the butterfly capacitor depicted in Fig. 14. The substrate is a 59-mil-thick microstrip substrate with a relative dielectric constant of 4.3. Due to the symmetry of the structure, only $S_{11} = S_{22}$ and $S_{12} = S_{21}$ have to be considered. The layout parameters are: 1) $p_1 = \theta$, the opening angle of the radial stub, with $20^\circ \leq \theta \leq 60^\circ$ and 2) $p_2 = R$, the radius of the stub, with 100 mil $\leq R \leq$ 500 mil. The frequency ranges between 0.5–7 GHz. We now prescribe an error limit of -45 dB. To obtain a convergent model, it turns out that 144 data points are needed. Their distribution is shown in Fig. 15. The validity of the model was tested in 416 randomly distributed data points for 25 discrete frequencies. For 99.1% of the tested points, the desired error limit of -45 dB was obtained.

In our last example, we consider the design and optimization of a Chebyshev low-pass filter specified as: 1) *passband*: from dc to 3.2 GHz with 1-dB maximum attenuation and 2) *stop-*

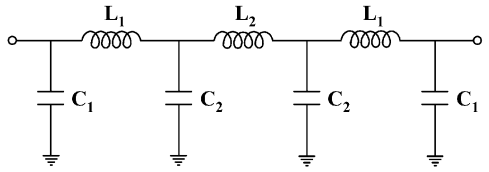

Fig. 16. Circuit equivalent of the seventh-order Chebyshev filter.

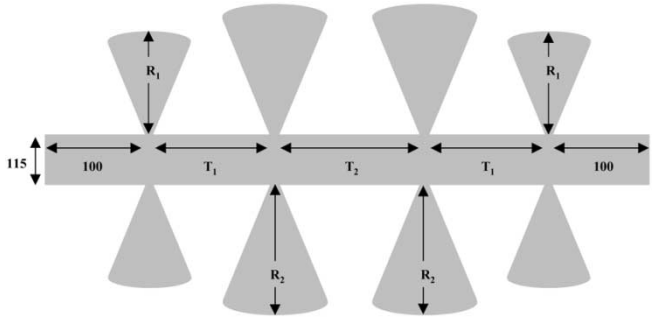

Fig. 17. Total filter layout corresponding to the circuit equivalent of Fig. 16 (all dimensions are in mils; microstrip substrate with thickness 59 mil and $\varepsilon_r = 4.3$).

band: from 3.9 to 7 GHz with at least 25-dB attenuation. This filter is realized on the same substrate as the butterfly capacitor discussed above. As our starting point, we select a seventh-order Chebyshev filter with a cutoff frequency of 3.2 GHz and with a 0.5-dB ripple in the passband. The predicted attenuation in the stopband is slightly lower than 25 dB, but the seventh-order filter is much more compact than its ninth-order alternative. Fig. 16 shows the circuit equivalent of the filter. The lumped-element values that yield the corresponding seventh-order filter behavior are: 1) $L_1 = 3.1965$ nH; 2) $L_2 = 3.4136$ nH; 3) $C_1 = 1.7227$ pF; and 4) $C_2 = 2.6141$ pF. The next step is to translate this circuit representation to an actual layout on the microstrip substrate. The inductors are realized as pieces of 50-Ω transmission lines. The exact lumped-element values can only be realized at a single frequency. We take this frequency to be 3.2 GHz. This implies that the width of the lines is 115 mil and that the line lengths corresponding with L_1 and L_2 become $T_1 = 292.3$ mil and $T_2 = 302.5$ mil, respectively. For the capacitors, we take the butterfly capacitors discussed above. The opening angle θ is kept constant at 45°. To obtain the wanted capacitance values C_1, C_2, respectively, the corresponding radii (at 3.2 GHz) are $R_1 = 237.4$ mil, $R_2 = 274$ mil, respectively. The values for these radii are derived from the MAPS-EMDB model of the butterfly capacitor. The total filter layout is shown in Fig. 17. Note the 100-mil port lines added at the input and output sides. Now, the filter response must be calculated over the whole dc–7-GHz range. Results (full line: before optimization) are displayed in Fig. 18(a) for the passband and in Fig. 18(b) for the stopband. The passband results do not comply with the defined goal (attenuation less than 1 dB). This is also the case in parts of the stopband where the attenuation is less than 25 dB. We now perform an optimization step by allowing T_1, T_2, R_1, and R_2 to vary. Table I lists the starting values together with their optimized counterparts.

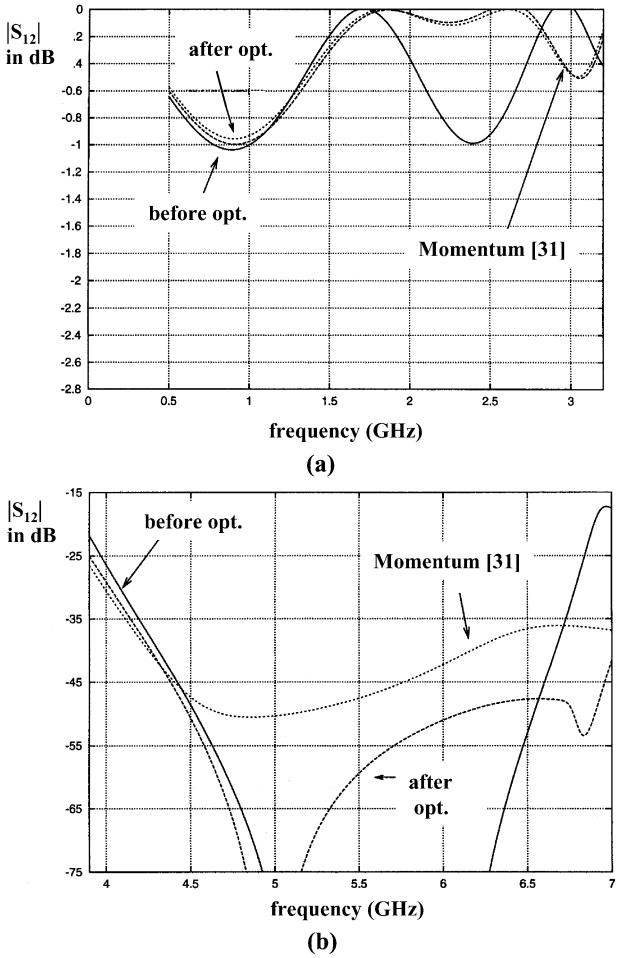

Fig. 18. $|S_{12}|$ as a function of frequency for the filter of Fig. 17. (a) Results for the passband ($0 \leq f \leq 3.2$ GHz). (b) Results for the stopband ($3.9 \leq f \leq 7$ GHz).

TABLE I
START VALUES AND OPTIMIZED VALUES FOR THE FILTER OF FIG. 17

	start	optim.
T_1	292.3	355.4
T_2	302.5	271.7
R_1	237.4	216.1
R_2	247.9	283.3

The filter response corresponding with the optimized layout parameters is also shown in Fig. 18 (dashed line: after optimization). This optimized result fully satisfies the prescribed criteria. To complete the picture, we have also calculated the EM results obtained by simulating the complete filter with a full-wave solver (*Momentum* from Agilent Technol.) (dashed line: *Momentum*). In the passband, the circuit simulator results based on the MAPS-EMDB models agree very well with the full-wave results. This is less the case in the stopband and increasingly so for higher frequencies. It is clear that the separate models for the capacitors and inductors do not account for the presence of field coupling between the different parts of the filter, which increases with frequency.

V. Conclusions

In this paper, it has been demonstrated that the integration of circuit optimization and full-wave EM analysis for planar circuits has much progressed. By allowing the EDA-tool user to introduce GLCs into a netlist and by fully automatically linking this new type of netlist element with an EMDB for the S-parameters of the GLC, a seamless integration of full-wave EM results into the circuit simulator is realized. The optimization process preserves its full flexibility (dc, ac, harmonic balance, envelope analysis, ...) and can now easily combine optimization of lumped elements together with geometrical layout parameters. Finally, we have discussed two approaches to generate a GLC–EMDB model: an on-the-fly-type approach and an up-front type of approach. Both approaches are designed to generate S-parameter data with a preset error limit over a user-defined multidimensional space of layout parameters over a broad frequency range and this with a minimal number of costly EM simulations.

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